AMENDMENT TO THE DRAWINGS

Please find enclosed replacement sheets for Figs. 1, 2, and 3 for the approval of the Examiner.

REMARKS/ARGUMENTS

This submission accompanies an RCE and serves as a response to the Final Office Action of March 9, 2006 issued in connection with the instant application. A Petition for Extension of Time (three months) and the fee therefor are submitted herewith.

The drawings have been objected to in paragraphs 5-8 of the Office Action. Reconsideration of the rejection is respectfully requested.

In order to overcome the objections in paragraphs 5-7 of the Office Action, replacement sheets for Figs. 1, 2, and 3 are enclosed herewith for the approval of the Examiner.

With regard to the objection to Fig. 8 (paragraph 8 of the Office Action), the Applicant respectfully traverses the objection. In particular, the Examiner alleges, in lines 3-5 of paragraph 8, that, "This is contrary to the teachings in the disclosure wherein the IAD is column addressing and EAD/LAD is row addressing." On the contrary, IAD and LAD both include row addresses and column addresses, (see specification, page 23, lines 14-24). Furthermore, the Examiner alleges that, "the IAD under EAD=(2, 0) should be (2, 0,), (2, 1), (2, 2) and (2, 3)," (Office Action, paragraph 8, line 6). However, such an IAD for such an EAD indicates a method of generating an internal address obtained by sequentially increasing the value of the second entry in the external address. Such a method is nowhere disclosed in the application and, in particular, is not included in the methods set forth on page 17, lines 7-18 of the specification.

The disclosure has been objected to for various informalities. Reconsideration of the objection is respectfully requested.

Applicant has appropriately amended the specification and Figs. 1-3 to overcome the grounds of the objection, except that, as previously explained, Applicant traverses the Examiner's conclusion that the IAD for EAD=(2, 0) should be corrected to (2, 0,), (2, 1), (2, 2) and (2, 3), as set forth in paragraph f and i, (Office Action, page 5, lines 18-20; page 6, lines 8-10).

Claims 1, 5, and 7 have been objected to. Reconsideration of the objection is respectfully requested. Claims 1 5, and 7 have been amended to overcome the objection.

Claim 1 was rejected under 35 U.S.C. §112, second paragraph. Reconsideration of the rejection is respectfully requested. Claim 1 has been amended to overcome the rejection.

Claim 2 was rejected under 35 U.S.C. §112, second paragraph. Reconsideration of the rejection is respectfully requested. Claim 2 has been amended to overcome the rejection.

Claim 3 was rejected under 35 U.S.C. §112, second paragraph. Reconsideration of the rejection is respectfully requested. Claim 3 has been amended to overcome the rejection.

Claims 1, 2, 4-6, 8, and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kazuyuki, Japanese Patent Application No. 07-078495, in view of Haraguchi et al., U.S. Patent No. 6,650,583. Reconsideration of the rejection is respectfully requested.

Independent claims 1 and 5 have been amended to provide that, "a first data generating method of generating the n bits of the internal write data ... [is] consecutively generating n number of values of '1'." In contrast, the Examiner admits that Kazuyuki only teaches "a fourth data generating method of alternately repeating the values '0' and '1' in this order (see Example, line 11)," (Office Action, page 11, lines 4-5).

With regard to Haraguchi et al., it nowhere teaches, discloses, or suggests a data generating method of generating n bits of internal write data being consecutively generating n number of values of "1."

Since each of claims 2, 4, 6, 8, and 9 is directly dependent upon one of independent claims 1 and 5, each of claims 2, 4, 6, 8, and 9 is allowable over Kazuyuki in view of Haraguchi et al. for the same reasons recited above with respect to the allowability of independent claims 1 and 5 over Kazuyuki in view of Haraguchi et al.

Claims 3 and 7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kazuyuki in view of Haraguchi et al., and further in view of Nomura et al., U.S. Patent No. 6,907,555. Reconsideration of the rejection is respectfully requested.

Since each of claims 3 and 7 is directly dependent upon one of independent claims 1 and 5, each of claims 3 and 7 is allowable over Kazuyuki in view of Haraguchi et al. for the same reasons recited above with respect to the allowability of independent claims 1 and 5 over Kazuyuki in view of Haraguchi et al.

With regard to Nomura et al., it nowhere teaches, discloses, or suggests a data generating method of generating n bits of internal write data being consecutively generating n number of values of "1."

In view of the foregoing amendments and remarks, allowance of claims 1-9 is respectfully requested.

Accordingly, the Examiner is respectfully requested to reconsider the application, allow the claims as amended and pass this case to issue.

Respectfully submitted,

THIS CORRESPONDENCE IS BEING SUBMITTED ELECTRONICALLY THROUGH THE UNITED STATES PATENT AND TRADEMARK OFFICE EFS FILING SYSTEM ON SEPTEMBER 11, 2006

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